Attorney Docket No. 03692.P007XD4

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	
RUMENNIK, et al.	Examiner: Hu, Shouxiang
Serial No.: 09/961,229	Art Unit: 2811
Filing Date: September 20, 2001	
For: HIGH-VOLTAGE TRANSISTOR WITH MULTI-LAYER CONDUCTION REGION	

Declaration Under 37 C.F.R. § 1.132

Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

I, Vladimir Rumennik, declare that:

1. I received the equivalent of a Masters of Science Degree in Electrical Engineering from The Institute of Steel and Alloys (Semiconductor Faculty) of Moscow, Russia in 1969. I also received the equivalent of a degree of Doctor of Philosophy in Electrical Engineering from the Institute of Physics and Engineering of Moscow, Russia in 1974.

2. From 1977 through 1979 I was employed as a Senior Device Engineer at International Rectifier Corporation of El Segundo, California, where I was a coinventor of a high power MOSFET device (commonly known as the HEXFET). One of the most fundamental transistor devices in use today, the HEXFET is described in U.S. Patent Nos. 5,008,725 and 5,130,767, both of which list me as

a named inventor.

3. I also worked at Xerox Corporation's Microelectronic facility in El Segundo, California from 1979 to 1983. At the end of 1983, I joined North American Phillips Corp. as the Department Head of their Microelectronics Research Department, supervising about 30-40 engineers in the development of high voltage power semiconductor devices. In 1988, I transferred to the Sunnyvale, California division of Phillips, called Signetics, where I managed a team of about 10 engineers working on high voltage integrated circuits.

4. I joined Power Integrations, Inc., in 1990, and since 1991 was Vice-President of Technology where I supervised approximately 15 engineers responsible for the development of new types of high voltage transistor devices and related technologies. I retired from Power Integrations in 2001.

5. During my career as an engineer and researcher I have worked with and managed dozens of students, scientists, and engineering professionals on numerous projects related to high voltage field-effect transistor devices, power integrated circuits, other power devices, and power integrated circuit manufacturing processes. I am named as an inventor on 17 granted U.S. patents. As a result of my professional experience, I am familiar with the skill of an ordinary person working in the field of high voltage transistor devices, high voltage circuits, and semiconductor processes for manufacturing high voltage devices as of 1996. I am also familiar with the state-of-the-art in these related fields extending across the time period from 1977 to the present.

6. Donald Disney, J.S. Ajit, and I are the coinventors of the subject matter of the above-captioned patent application, which is a divisional of U.S. Serial No. 09/574,563, now U.S. Patent No. 6,570,219, which is a divisional of U.S. Serial No. 09/245,030, now U.S. Patent No. 6,207,994, which, in turn, is a continuation-

in-part of U.S. Serial No. 08/744,182, now abandoned. As a coinventor, I am familiar with the subject matter of that application and the invention defined by pending claims 93-111, as amended. I have also read and am familiar with U.S. Patent No. 5,386,136 of Williams et al. (hereafter "Williams"); the English translation of JP404107877A of Yamanishi et al. (hereafter "Yamanishi"); U.S. Patent No. 5,313,082 of Eklund (hereafter "Eklund"); and U.S. Patent No. 4,626,879 of Colak (hereafter "Colak").

7. I have also read the Final Office Action dated August 20, 2003 for the above-captioned patent application and understand that claims 93-111 stand rejected under 35 U.S.C. § 103(a) as being unpatentable Williams in view of Yamanishi and/or Eklund. Additionally, I understand that claims 96-98 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Williams in view of Yamanishi and/or Eklund, and further in view of Colak.

8. Ever since I began working on power devices in the semiconductor industry more than twenty years ago there has existed a pressing need for a high voltage transistor device capable of sustaining a very high breakdown voltage (V_{bd}) combined with a low specific on-resistance (R_{sp}), which is the product of on-state resistance and surface area. A lower R_{sp} allows a smaller HVFET transistor to be used to meet the on-state resistance requirements of a given application, which reduces the area and, respectively, the cost of the power integrated circuit. For example, throughout the 1980s and early 1990s semiconductor manufacturers repeatedly failed in their attempts to produce a power transistor device that can reliably sustain several hundred volts in the off-state, yet conduct with relatively low resistance in the on-state. Companies such as Phillips, Siliconix, Power Integrations, Motorola, and various Japanese companies including Matsushita Electronic Company (known as MEC) Inc., fell short in their attempts to produce a high voltage field-effect transistor with a breakdown

voltage on the order of several hundred volts and a very low R_{sp}. Up until the time of our invention the prior art generally consisted of device structures that suffered from high specific on-resistance and/or relatively low breakdown voltage.

9. Around 1990, Power Integrations began collaborating with Matsushita Electronic Company of Japan to develop new high voltage technologies. Under the parties' agreement, Matsushita was to implement the processes and device structures developed by the engineers working under my direction at Power Integrations. Yamanishi-san (the named inventor of the Yamanishi reference) was one of the Matsushita engineers who gained knowledge of Power Integrations' high voltage transistor device structures and also learned from Power Integrations how to fabricate high voltage field-effect transistors (HVFETs) through his participation in this technology exchange. At that time, the state-of-the-art was characterized by a device structure having an n-type extended drain region with a p-type top layer. It was known, for example, that this structure approximately doubled the charge in the JFET channel below the top layer, thereby lowering the R_{sp}. Because this top layer helps to deplete the extended drain when the extended drain is supporting a high voltage, a relatively high breakdown voltage could be also be maintained despite the increased charge density.

10. Sometime in 1991, Yamanishi-san proposed utilizing the technique of dopant segregation to try to change the conductivity type at the substrate surface in order to further improve the transistor's high-voltage operating characteristics. The technique of dopant segregation, whereby a thermal oxidation cycle is used to remove dopants from the underlying semiconductor material, was well known in the semiconductor processing arts in 1991. It was equally well understood, however, that the technique of dopant segregation was a highly unpredictable

technology, making it very difficult to control the resultant impurity doping concentration in the various silicon layers affected. For this reason, ordinary practitioners in the semiconductor arts at that time – that is, someone with an engineering degree and 1-2 years experience in the industry – would have considered it practically impossible to achieve a working HVFET having a conductive top layer utilizing Yamanishi's method of first forming an extended region by diffusion, followed by implantation of boron ions for impurity doping of the P-type region and heat oxidation of the surface of the substrate. In my opinion, an ordinary engineer working in the high voltage device field would not have attempted to fabricate a HVFET with a top conduction layer according to Yamanishi's teachings because such a person would have lacked any reasonable expectation of success. In other words, a person of ordinary skill in the art would have understood that Yamanishi's approach is so unpredictable that creating a working high-voltage field-effect transistor with an extended drain structure having dual conduction channels would be impractical.

11. By way of example, when Yamanishi-san first proposed an HVFET formed using dopant segregation at the upper surface of the extended drain, engineers at Power Integrations simulated a HVFET fabricated according to Yamanishi-san's approach to determine if we could make it work. The shape of the boron distribution inside silicon is determined by basic physics laws of impurity diffusion in solid silicon and can be expressed in terms of diffusion and segregation coefficients. We found that we could not make such a device work as intended, even though we had great financial incentive to do so. Accordingly, we rejected Yamanishi-san's approach as impractical and decided to pursue alternative approaches to achieving an improved high voltage field-effect transistor.

12. To my knowledge, neither Matsushita nor any other semiconductor

manufacturer was ever able to achieve a working HVFET having a top conduction layer fabricated according to Yamanishi's method of dopant segregation, or any other alternative approach. To the best of my knowledge, despite numerous attempts by many semiconductor companies over the course of more than a decade, no manufacturer of high-voltage semiconductor devices was able to produce a HVFET having dual conduction channels in an epitaxial layer that functions as an extended drain region. That is, it was not until the date of our invention that a high-voltage transistor device structure included first and second conduction channels respectively disposed above and below a buried region of opposite conductivity type. For instance, engineers in the semiconductor industry struggled throughout the years from 1991 -1996 to try to achieve such a device structure, but could not do so. I believe that our invention is the first apparatus to make this long sought after goal a practical reality.

13. Based on my knowledge of high voltage semiconductor devices and the experimental simulation results we ran in the early 1990s, the device structure taught by Yamanishi is inoperable due to the lack of adequate charge (i.e., impurity dopant concentration) in the top n-type layer. Indeed, due to the unpredictability of the segregation processing technique, it is doubtful that an n-type channel could be reliably produced in his device. Because the segregation technique was widely known to be unpredictable and uncontrollable, in my opinion a person of ordinary skill in the semiconductor arts would have rejected Yamanishi's approach as having no reasonable chance of success to produce a HVFET having a top conduction channel. Moreover, due to the deficiencies in his approach, in my estimate the Yamanishi reference fails to teach or suggest our HVFET invention; that is, a high voltage field-effect transistor with an extended drain structure having dual JFET-type conduction channels. In my opinion,

Yamanishi does not disclose the formation of a top conduction layer, and one would not be inherently formed from his processing approach.

14. I also believe that it would have been beyond the skill of an ordinary practitioner in 1996 to depart from Yamanishi's teaching and devise an alternative method for forming a buried layer with associated above and below JFET-type conduction channels, as achieved in our invention. The reason why is because it was no one was able to achieve a true top conduction channel with sufficient charge until the date of our invention. Neither Williams, nor any other prior art reference that I know of teaches how to attain an HVFET with upper and lower JFET conduction channels.

15. In my opinion a person of ordinary skill in the semiconductor arts in 1996 would not have had a reasonable expectation of success in combining the references in the manner suggested by the examiner in the Office Action dated August 20, 2003. Based on my experience working in this field, a person of ordinary skill would understand Williams as teaching the formation of an N-type drift region having a depth less than one micron below the surface of the substrate. The reason why is because this shallow N-type drift region is shown in the figures as having the same depth as the N+ drain diffusion region, e.g., region 507 in Figure 5. In 1996, as of the filing date of our original application, it was also a standard practice in the semiconductor industry to form the N+ drain diffusion region of a power MOSFET device to a depth less than approximately 1.0 micron. Williams' teaching of forming an extended drift region with a depth less than one micron would have discouraged one of ordinary skill in the art to make a modification or combination with Yamanishi and/or Eklund to arrive at our claimed invention. The reason why is because an ordinary practitioner attempting to combine Williams with Yamanishi and/or Eklund would have understood that a one micron deep N-type drift region is too shallow to permit formation of a buried

region therein using Yamanishi's method of segregation of dopants by heat treatment, or Eklund's formation of a p-type JFET gate control layer that contacts drain diffusion region within a diffused n+ well.

16. In my opinion, a person of ordinary skill would also have concluded that Williams could not be reasonably combined with Eklund to produce a device structure having conduction channels above and below a buried region disposed in an epitaxial layer, wherein the buried region is spaced-apart from the drain diffusion region, because of the fundamental differences between Williams' and Eklund's fabrication methods and resulting device structures. For example, whereas Williams forms a shallow drift region in an epitaxial layer, Eklund teaches the formation of a well region in a substrate, a JFET gate control layer that contacts a drain diffusion in the well region, followed by the formation of a separate top layer above the gate control layer.

17. Additionally, a person of ordinary skill in the art would have lacked motivation to combine Yamanishi with Williams to produce a device structure that includes dual JFET-type conduction channels above and below the buried region because such a person would have had no reasonable expectation that Yamanishi's segregation approach for trying to form a top n-type region would work.

18. Based on prior simulation test results and my knowledge of the skill level of ordinary practitioners working in the semiconductor arts in 1996, it is my further opinion that there would have been no apparent reason for a person of ordinary skill to combine or modify Yamanishi and/or Eklund with Williams because I believe that the person of ordinary skill would have performed the same simulations that we did and concluded that the resulting device would not work for its intended purpose.

19. In my further opinion, the lateral double-diffused MOS transistor device structure and method taught by Colak is so completely different than Yamanishi, Eklund and Williams that a person of ordinary skill in the semiconductor arts would not have been motivated to modify or combine Colak with the other cited references so as to arrive at our invention. For instance, even though Colak shows an n+ layer 24a separated from an n+ lower layer 14 by a p+ layer 16, he specifically teaches in column 5, lines 52-62 that layer 14 is isolated from the current-carrying path due to the intervening second semiconductor layer 16.

20. I wish to stress the point that in the highly competitive semiconductor industry, although high voltage device structures with various extended drain structures were well known in the field, as well as the desirability of producing a transistor with reduced lower R_{sp} and high breakdown voltage, the semiconductor industry failed for years to develop a reliable high voltage MOSFET with a top conduction channel in the extended drain region. In my opinion, the fact that no one arrived at the combined features which are incorporated in the present invention is a strong indication that our invention would not have been obvious to one of ordinary skill in the art at the time our invention was made.

21. I declare, to the best of my knowledge, that all statements made in this document are true, and that all statements made on information and belief are believed to be true; and further, that these statements are made with the knowledge that willful false statements are punishable by fine or imprisonment, or both, under §1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of above-captioned application or any patent issued thereon.

Date: November 12, 2003

Vladimir Rumennik